REMARKS

New claims 21-26 have been added so that claims 1-26 now appear in this application for the Examiner's review and consideration. Claims 1-20 remain as originally filed.

Claims 1-9 and 15 were rejected as being unpatentable over Akiyama et al. (U.S. Patent 6,680,260).

Claim 1 recites a method for reducing roughness on a free surface of a semiconductor wafer by applying a rapid thermal annealing process under a pure argon atmosphere. In contrast, Akiyama teaches to eliminate crystalline defects (COPs) within a silicon single crystal wafer using a two step process. The standard silicon wafer has been cut from an ingot and polished or otherwise treated (See Akiyama, col. 11, line 65 to col. 12, line 9) before the disclosed process is used. The final surface roughness of such a wafer is already at a minimum value according to standard industry practice. The first step of Akiyama's process is to anneal in a range of 1100° C to 1300° C in Argon gas for more than one minute to out-diffuse oxygen in the crystal and rid the oxide film inner wall of void defects. This results in forming a low-defect layer. The second step is to anneal in an oxidizing atmosphere at a temperature of 700° C to 1300° C for one minute or more to form an oxide film, to interject interstitial silicon and to eliminate void defects to a deep part of the crystal. Operating in this manner effectively eliminates COPs from the surface to a depth of about 5 to 10 μm or more (See Akiyama, col. 12, lines 19-35). Consequently, the thermal treatments disclosed by Akiyama are not for reducing surface roughness, and there is no suggestion or teaching in Akiyama that could lead one skilled in the art to expect reduction of surface roughness from the process steps that are conducted after the ingot is polished. In fact, as explained above, Akiyama's two step process focuses on eliminating COPs and is not directed to reducing surface roughness. The Applicants therefore respectfully submit that Akiyama cannot anticipate claim 1.

Dependent claim 2 includes the further steps of, prior to conducting rapid thermal annealing, implanting atoms under a face of a donor substrate to form a zone of weakness, bonding a stiffening substrate to the face, and detaching the donor substrate along the zone of weakness to form the wafer including the stiffening substrate and a useful layer. In contrast, Akiyama teaches to implant at least one of hydrogen ions and rare gas into the surface after implementing his two-step heat treatment process (See col. 3, lines 3-22 and col. 13, line 66 to col. 14, line 6). Thus, claim 2 is patentably distinct over Akiyama.

Dependent claim 3 recites rapid thermal annealing at a high temperature dwell in the range of about 1000°C to 1400°C, for a period in the range of about 1 second to 60 seconds, and dependent claim 4 recites that the high temperature dwell is in the range of about 1100°C to 1250°C, for a period in the range of about 5 seconds to 30 seconds. In contrast, Akiyama teaches to use two separate heat treatments that are each greater than one minute (See col. 12, lines 22-19). Thus, claims 3 and 4 are patentably distinct over Akiyama.

Claims 1-4 recite conducting the recited steps to achieve a particular result. As Akiyama is not concerned with using such steps to achieve the result, his disclosure does not anticipate or render obvious the subject matter presently claimed in claims 1-4.

Claims 5-9 and 15 all directly or indirectly depend on claim 1, which is patentably distinct from Akiyama as explained above. Thus, these claims should be allowable for at least the same reasons. In view of the above remarks, the Applicants respectfully request withdrawal of the 35 U.S.C. 103(a) rejections of claims 1-9 and 15.

Claims 16-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy (U.S. patent 5,856,027) in view of Thakur et al. (U.S. patent 5,738, 909).

Murphy is directed to thermal barrier coating systems for nickel-based and cobalt-based superalloys, for use in a gas turbine engine (See col. 2, lines 14-17). The cited verbiage at col. 6, lines 34-41 pertains to forming an alpha aluminum layer on a bondcoat coated specimen, and is not a method for reducing surface roughness of the free surface of a semiconductor wafer.

Thakur discloses a method of forming thin oxides by heat treating a substrate in an atmosphere containing oxygen, and then using an Argon ambiance during a cool down phase to prevent the wafer from being contaminated during the cooling period (see col. 6, lines 18-16). Like Murphy, Thakur does not suggest or teach a method for reducing surface roughness of a free surface of a wafer of semiconductor material. In fact, the introduction of an Argon atmosphere in the process chamber during cool down would not result in reducing the surface roughness because at this time in the process the wafer has an oxide surface that cannot be smoothed using thermal annealing. Furthermore, the temperature in the chamber is not high enough and does not last for a sufficiently long enough time to allow surface smoothing.

The Applicants respectfully assert that there is no suggestion or teaching to combine the thermal barrier coating systems of Murphy with the method of forming ultrathin oxides as taught by Thakur. Moreover, even if the references were combined, the present invention would not be the result as neither reference, alone or in combination, discloses

utilizing a pure Argon atmosphere during an annealing process as recited in claim 16 to reduce the surface roughness of a free surface of a semiconductor wafer. Thus, claim 16 is patentably distinct thereover. Claims 17-20 all directly depend on claim 16, which is patentably distinct over the cited art. Thus, claims 17-20 should be allowable for at least the same reasons. In view of the above comments, the Applicants respectfully request withdrawal of the 35 U.S.C. 103(a) rejections of claims 16-20.

Applicants appreciate the indication of allowable subject matter in claims 10-14 and the notation that those claims would be allowed if rewritten in independent form to include all of the recitations of the base claim and any intervening claims. In view of the preceding remarks, as claims 1-8 and 15-20 are believed to be allowable, Applicants see no need to re-write claims 10-14 in independent form.

Finally, new independent claim 21 recites a method for reducing roughness on a free surface of a semiconductor wafer that includes a rapid thermal anneal followed by polishing and at least one additional treatment step after the polishing step to enhance smoothness and to reduce slip lines in the free surface of the wafer. Support for claim 21 can be found, for example, on page 10, lines 10-15 of the application and in prior claims 10-14. No new matter has been added. Such a process is believed to be patentably distinct over the cited art for the same reasons as claims 10-14. Furthermore, dependent claims 22-26 should also be allowable for at least the same reasons.

In view of the above, the entire application is believed to be in condition for allowance, early notification of such would be appreciated. Should the Examiner not agree, a personal or telephonic interview is respectfully requested to discuss any remaining issues in order to expedite the eventual allowance of the claims.

Respectfully submitted,

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Date

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